2.9 A Fractional-N PLL for SONET-Quality Clock-Synthesis Applications

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Traditionally precision clock sources have been implemented by using precision resonators such as quartz crystals or SAW resonators. In high-performance PLLs, VCXOs or voltage-control SAW oscillators (VCSOs) have been used. These implementations rely on the ability to accurately manufacture a precise resonator for a given frequency, using simple circuitry to entice the oscillation. It is much easier from a manufacturing-flow and process-control perspective to fabricate low-accuracy (but high-Q) fixed-frequency resonators, but this places the difficulty in the frequency synthesis. Fractional-N PLLs are a well-known technique to synthesize frequencies with arbitrary precision from a fixed-frequency reference clock. This property makes them attractive for use with fixed timing sources such as crystal oscillators and VCXOs. While the basic idea is simple, the key to a successful implementation of a frequency synthesizer is in managing jitter and spurious performance. The SONET standard, for example, has some of the most stringent jitter requirements for clock sources. A frequency-synthesis IC targeted to replace high-frequency XO and VCXOs is proposed. Jitter performance in the OC-192 band, integrated from 50kHz to 80MHz, is $0.3ps_{rms}$ and the current draw excluding the output driver is 70mA.

An overview of the chip architecture is shown in Fig. 2.9.1. A crystal oscillator produces a reference clock at a fixed frequency. In order to obtain a high reference frequency for better performance of the fractional multiplier, an overtone oscillator is chosen. This reference clock feeds a fractional-N loop. This loop uses a charge-pump-based phase detector feeding into a current-input ΔΣ ADC. A phase-error estimation is subtracted with a current output DAC [2]. A digital loop filter implements the integration path creating the zero in the transfer function [1]. A DAC controls the frequency of the VCO [1]. The VCO frequency is divided by an integer to produce the output frequency and by a phase-select divider [3] to produce the feedback. The phase-select divider is controlled by a ΔΣ modulator. The input to this modulator is the digital fractional number M, and the output is a sequence of integers approximating M. To implement an XO of arbitrary frequency, M is a constant. To implement a VCXO, M is a constant plus the output of a ΔΣ ADC that converts a control voltage.

In order to achieve good jitter performance in a fractional-N loop, a good VCO is required. But in order to achieve good spurious performance of the LC oscillator, a shield is implemented, reducing the Q of the inductor. At low and medium frequency the phase-noise performance of a crystal oscillator is far better than that of an LCVCO. So the goal is to extend the bandwidth of the loop somewhat to reduce the overall noise. Unfortunately, the wider bandwidth reduces the effective oversampling ratio between update rate and loop bandwidth, making quantization error a much bigger noise contributor. Also, the noise and linearity performance of the phase detector become more significant.

The phase detector, shown in Fig. 2.9.2, is implemented as a modified up/down/reset phase detector. Typically such a phase detector exhibits crossover distortion, because multiple current sources determine the phase to charge gain. Another source of nonlinearity in phase-to-charge conversion is the speed of the reset circuitry near crossover and possible crosstalk between the 2 inputs through the power supply.

By creating a delay larger than the noise-shaped phase error when in lock and using this delay to create *upd* and *downd* signals, then logically combining *up* and *downd* and *down* and *upd* to drive the charge pump, it is guarantee that in lock, a certain sequence of events is achieved which avoids zero crossings. Also, a fully differential output current is created. Acquisition of lock is still guaranteed, because the PFD works in a way similar to the traditional textbook implementation.

The known technique of estimating quantization error and injecting it into the phase detector is applied here [2]. Figure 2.9.3 shows the relevant blocks. As a by-product of integrating the M value minus the actual divide value, the output of the first integrator of the ΔΣ modulator calculates the expected phase error (no extra hardware required). This value, D, has to be converted into a charge, Qa, that matches the charge, Qcp, we expect from the charge pump. Specifically,

$$Qcp = \Delta\Phi \cdot t_{VCO} \cdot I_{cp} = Qa = t_{DAC} \cdot D \cdot I_{ref}$$

Therefore, I_{cp} and I_{ref} should be derived from the same source. t_{DAC} must be a time related to t_{VCO} (in our case 4 cycles), so that matching to about 5% can be achieved. The DAC implementation has 128 identical elements and 2 scaled sources. A return-to-zero constraint reducing nonlinearity is inherent in the operation. DEM linearizes the output current.

In order to reduce the noise contribution from the phase-detector ADC (Fig. 2.9.4), a small full-scale value is chosen, thereby reducing quantization error. The full scale is actually less than the peak input phase error expected. This is possible because a low-pass signal transfer function is built into the ADC. The first input capacitor serves as a current summing node as well as part of the lowest frequency pole of the ADC signal transfer function. More substantial noise shaping is achieved by the 2 integrators that follow. A large nonlinear capacitance is present at the input to the current ADC. This capacitance is due to the charge-pump current sources and the DAC current sources. Unlike an RC filter in front of the ADC, embedding the LPF function in the ADC holds the nonlinear capacitance at virtual ground, removing its effect.

Phase-noise plots of the system in 5 different modes are shown in Fig. 2.9.5. Regions of dominant noise sources are identified: XO, PD, VCO, PE (noise shaped phase error), OD (output driver), and VCADC (input ADC). The first (nopec38) shows the performance using 38MHz update rate and no phase-error cancellation. The second curve (pec38) shows how phase-error cancellation can reduce the PE noise dramatically. Tripling the update rate to 114MHz lowers the PD contribution and pushes out the PE contribution (nopec114), which then can be cancelled by applying phase-error cancellation again (pec114), although the impact is less at this update rate. Finally, the ADC that implements the VCXO function is turned on (vc_pec114). Its noise is shown to dominate over the XO noise. The implemented gain is 180ppm/V.

Spurious performance is worst for an M value near an integer, such as 40.001. It will create spurs at $0.001 \times f_{xo}$. Additionally, if the output frequency produces terms near f_{xo} (for example by dividing f_{vco} by 8), the worst-case spurs occur at ~60dBc for a signal around 600MHz, as shown in Fig. 2.9.6. When choosing the exact crystal frequency, this is an important consideration. The low-frequency spurs at multiples of 60Hz are due to the test setup. The spurs at multiples of 7kHz are due to a mixing of the harmonics of the output frequency with harmonics of the crystal frequency at the crystal chip interface, whereas the spurs at 57kHz and above are created by non-linearity in the phase detector. The 80MHz spur is due to the presence of internal digital clocks.

The layout is shown in Fig. 2.9.7(a) with a die micrograph in Fig. 2.9.7(b) that shows a faraday shield over the inductor. The chip occupies $4mm^2$, the core draws 70mA, and the chip draws 110mA including an LVPECL output buffer. This paper demonstrates that frequency-synthesis technology can replace traditional oscillators even in high-performance applications.

References:

[1] Derrick Wei et al, "A Monolithic Low Bandwidth Jitter Cleaning PLL with Hitless Switching for SONET/SDH Clock Generation," *ISSCC Dig. Tech. Papers*, pp. 236-237, Feb., 2006.

[2] S. Parmati, L. Jansson, I. Galton, "A Wideband 2.4-GHz Delta-Sigma Fractional-N PLL with 1-Mb/s In-Loop Modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49-62, Jan., 2004.

[3] Bram De Muer and Michiel Steyaert, CMOS Fractional-N Synthesizers, Kluwer Academic Publishers, Chapter 3, pp. 53-82, 2003.

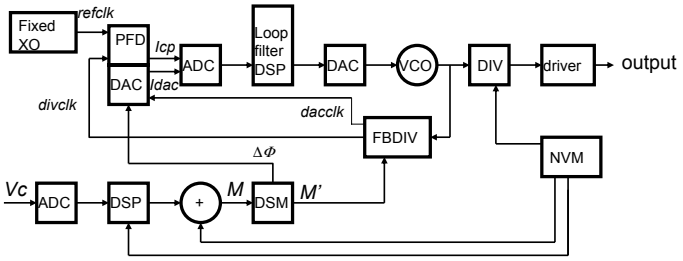

Figure 2.9.1: Block diagram.

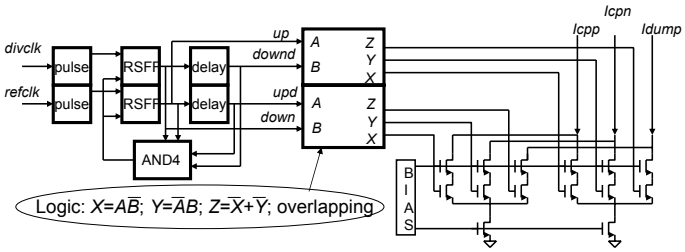

Figure 2.9.2: Phase detector.

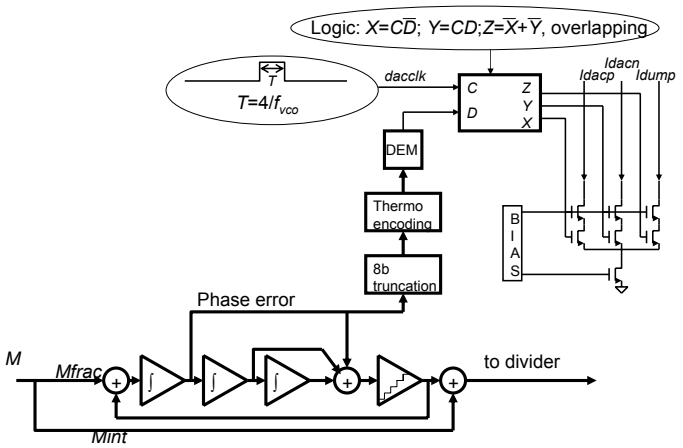

Figure 2.9.3: Phase error cancellation.

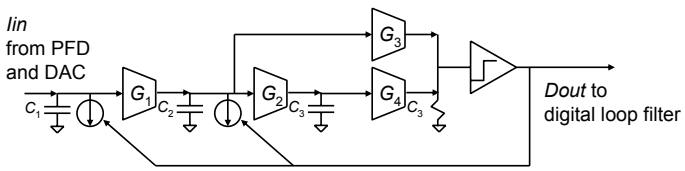

Figure 2.9.4: ADC architecture: dominant pole at $f=G_1/(2\pi.C_1)$.

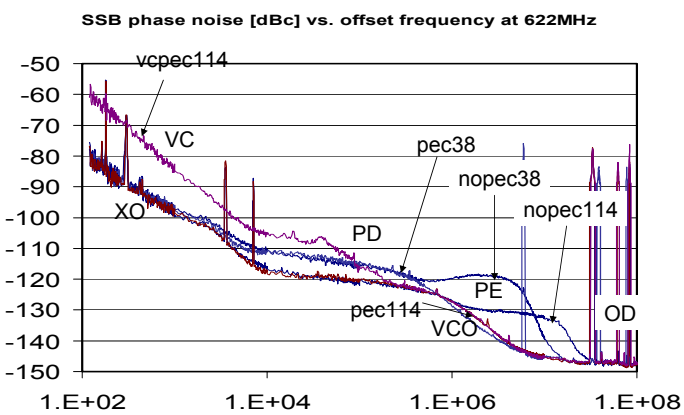

Figure 2.9.5: Phase noise performance for different operating modes. Noise contributors are identified.

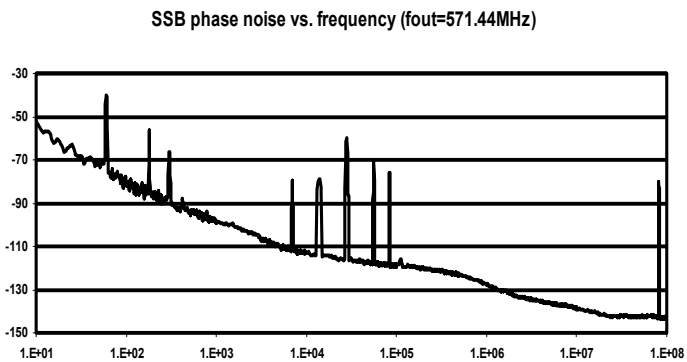

Figure 2.9.6: Spurious performance for M=40+1/1024.

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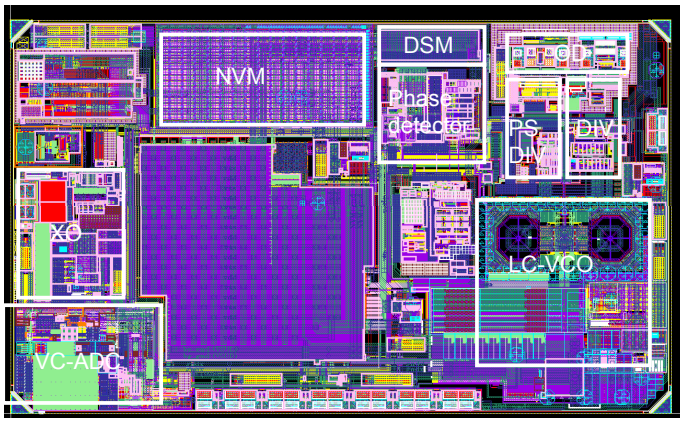

Figure 2.9.7(a): Layout.

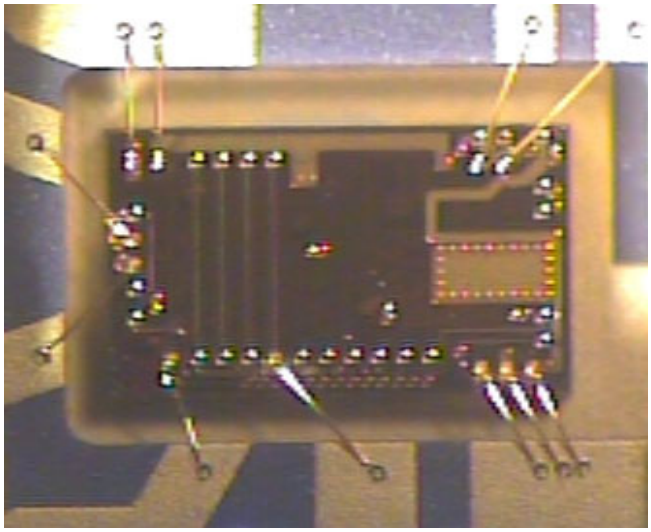

Figure 2.9.7(b) Die in standard ceramic crystal package.

OC-48 noise 12kHz to 20MHz	0.3ps$_{rms}$
OC-192 jitter 50kHz to 80MHz	0.3ps$_{rms}$
Core current excluding output	70mA
Total current VCXO 622MHz with LVPECL output	110mA
Process	0.13µm CMOS, thick metal, post processing
Die area	4mm^2

Figure 2.9.8: Table of results.

